WHAT IS CLAIMED IS:

1. A multiplication logic circuit for multiplying two n bit binary numbers, the circuit comprising:

array generation logic for performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combinations comprising an array of binary values;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the binary numbers;

wherein the array reduction logic comprises:

first array reduction logic comprising a plurality of binary counters, each for receiving the binary values of all binary numbers in a respective column of the array, and for outputting binary numbers; and

second array reduction logic having logic imposing asymmetric delays on inputs to the logic and for receiving the binary numbers output from the parallel counters at the inputs and for outputting said binary numbers to said addition logic.

2. A multiplication logic circuit according to claim 1, wherein said first array reduction logic includes adder logic for adding binary values of binary numbers in respective columns.

3. A multiplication logic circuit according to claim 2, wherein said adder logic comprises at least one full adder.

4. A multiplication logic circuit according to claim 2, wherein said adder logic is arranged to add binary values of binary numbers for columns in said array having 3 or less bits.

5. A multiplication logic circuit according to claim 1, wherein said second array reduction logic comprises any one of or combination of a full adder, a half adder, and four to two compressor logic.